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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/013,981	12/10/2001	Chia-Hui Han	JCLA7632	1935

23900 7590 10/17/2007

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EXAMINER	
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ART UNIT	PAPER NUMBER
2613	

MAIL DATE	DELIVERY MODE
10/17/2007	PAPER

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/013,981
Filing Date: December 10, 2001
Appellant(s): HAN, CHIA-HUI

Jiawei Huang
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 13 March 2006 and the summary of claimed subject matter filed 25 July 2007 appealing from the Office action mailed 15 June 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter filed 25 July 2007 is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

A substantially correct copy of appealed claims 1-14 appears on pages 13-16 of the Appendix to the appellant's brief. The minor errors are as follows: claims 1-3, 6-7 and 9-12 should have status identifier "(Previously presented)" instead of "(Previously amended)".

(8) Evidence Relied Upon

5,726,645	KAMON et al.	3-1998

6,008,735	CHILOYAN et al.	12-1999
6,185,620 B1	WEBER et al.	2-2001
6,426,820 B1	VERZULLI	7-2002

Admitted prior art

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-3 and 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Verzulli (U.S. Patent 6,426,820 B1) in view of Kamon et al. (U.S. Patent 5,726,645) or Chiloyan et al. (U.S. Patent 6,008,735).

Regarding claims 1, 6 and 8-11, Verzulli discloses in FIG. 1 a self-test arrangement for a remote control. FIG. 1 comprises a microcontroller for controlling the setting of a self test during which a IR transmitter transmits test data and the controller receives test data and compares received data with transmitted data to determine whether test is successful or not. The transmission of test data and receiving of test data occur concurrently. The difference between Verzulli and the claimed invention is that Verzulli does not teach to select a test brand name from a plurality of brand names. Kamon et al. teaches in col. 2, lines 60-66 that predetermined operation setting associated with manufacturers is stored in memory and retrieved by microprocessor for setting the transmitter. Similarly, Chiloyan et al. teaches in FIG. 3A through FIG. 3M to try various brand names for finding the correct setting of a remote control unit. One of ordinary skill in the art would have been motivated to combine the teaching of Kamon et al. or Chiloyan et al. with the remote control self-test arrangement of Verzulli because it allows the use of a single microcontroller to test infrared transceivers made by various manufacturers. Thus it

would have been obvious to one of ordinary skill in the art at the time the invention was made to store predetermined operational setting of transmitter of various manufacturers, as taught by Kamon et al. or Chiloyan et al., in the remote control self-test arrangement of Verzulli because it allows the use of a single microcontroller to test infrared transceivers made by various manufacturers.

Regarding claims 2 and 12, Kamon further teaches the steps of selecting brand names to serve as a test brand name are repeated until all brand names have been selected (see col. 7, lines 1-58).

Regarding claims 3 and 7, Verzulli teaches transmission and reception simultaneously.

Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Verzulli in view of Kamon et al. or Chiloyan et al. as applied to claims 1-3 and 6-12 above, and further in view of Weber et al. (U.S. Patent 6,185,620 B1).

Verzulli, Kamon et al. and Chiloyan et al. have been discussed above in regard to claims 1-3 and 6-12. The difference between Verzulli, Kamon et al. and Chiloyan et al. and the claimed invention is that Verzulli, Kamon et al. and Chiloyan et al. do not teach two groups of memory. Weber et al. teaches in FIG. 9A arrangement of system memory for a transmitter/receiver unit. Weber et al. teaches in FIG. 9A and col. 9, line 61-col.12, line 67 TX DATA, TX DMA and TX BUFFER for data to be transmitted and RX BUFFER, RX DMA and RX DATA for data that has been received. One of ordinary skill in the art would have been motivated to combine the teaching of Weber et al. and the modified self-test arrangement of Verzulli, Kamon et al. and Chiloyan et al. because this arrangement of memory facilitates memory management so that

memory will not be accidentally overwritten by other applications. Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to partition memory into two groups, one for receiving and one for transmitting, as taught by Weber et al., in the modified self-test arrangement of Verzulli, Kamon et al. and Chiloyan et al. because this arrangement of memory facilitates memory management so that memory will not be accidentally overwritten by other applications.

Claims 5 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Verzulli in view of Kamon et al. or Chiloyan et al. as applied to claims 1-3 and 6-12 above, and further in view of admission (admitted prior art FIG. 1 and FIG. 2).

Verzulli, Kamon et al. and Chiloyan et al. have been discussed above in regard to claims 1-3 and 6-12. The difference between Verzulli, Kamon et al. and Chiloyan et al. and the claimed invention is that Verzulli, Kamon et al. and Chiloyan et al. do not disclose that the infrared controller is enclosed within a South Bridge control chipset. However, FIG. 1 (prior art) of instant application teaches that infrared controller 100 is enclosed within a South Bridge chipset 400. South Bridge chipset is commonly used for connecting peripheral devices to the North Bridge chipset in a computer motherboard. One of ordinary skill in the art would have been motivated to combine the teaching of admission with the modified self-test arrangement of Verzulli, Kamon et al. and Chiloyan et al. to include the infrared controller within a South Bridge chipset for applications where the IR transceiver is a peripheral device because sharing a controller with other peripheral devices keeps the cost of a computer low while provides additional functionality. Thus it would have been obvious to one of ordinary skill in the art at the

time the invention was made to include the infrared controller as part of a North Bridge chipset for applications where the IR transceiver is a peripheral device of a computer, as taught by admission, in the modified self-test arrangement of Verzulli, Kamon et al. and Chiloyan et al. because sharing a controller with other peripheral devices keeps the cost of a computer low while provides additional functionality.

(10) Response to Argument

On page 5 of the Brief, the Appellant cites In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-1458 (Fed, Cir. 1998) and argues that the problems intended to be solved by **each prior art reference are not identical to that of the present invention**. First, Appellant cannot show non-obviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Second, the test for combining references is what the references as a whole would have suggested to one of ordinary skill in the art. *In re Sheckler*, 168 USPQ 716 (CCPA 1971); *In re McLaughlin*, 170 USPQ 209 (CCPA 1971); *In re Young*, 159 USPQ 725 (CCPA 1968). In this case, all the references applied in the rejections are directed to remote controller and from the same field of endeavor. Considering all these references as a whole, it would have already suggested to one of ordinary skill in the art to make the combination for trying settings of various brand names for identifying the particular brand name of an infrared transmission head under test.

Third, if it is obvious to combine references for one reason it is obvious to combine references for all reasons. In re Graf, 145 USPQ 197 (CCPA 1965); *In re Finsterwalder*, 168

USPQ 530 (CCPA 1971); *In re Knonig*, 539 F.2d 1300, 190 USPQ 425 (CCPA 1976). *In re Dillon*, 892 F.2d 1544, 13 USPQ2d 1337 (Fed. Cir. 1989); *In re Dillon* 919 F.2d 688, 16 USPQ2d 1897 (Fed. Cir. 1990). As recognized by the Examiner, in a 35 U.S.C. § 103 obvious type rejection, the problems solved by the references do not have to be identical to that of the present invention. Instead, obviousness is based on whether the skilled artisan, when confronted with the same problems as the inventor, would select the elements from the cited prior art references for combination in the manner claimed. There are three possible sources for motivation to combine prior art references, namely, nature of problem to be solved, teachings of prior art, and knowledge of persons of ordinary skill in the art. *In re Rouffet*, 47 USPQ2d 1453 (Fed, Cir. 1998).

The problems solved by the claimed invention can be interpreted broadly as:

Given an infrared transmission head, how to test the transmission head to see whether it meets certain functions according to different manufactures' specification; or

Given an infrared transmission head, without knowing its manufacturer or brand name, select a suitable setting, from a plurality of brand names, for driving the infrared transmission head.

Verzulli teaches in FIG. 1 a self-test arrangement for an infrared transceiver. It comprises a microcontroller with internal memory (ROM and RAM) and external memory (EEPROM) for controlling the infrared transceiver. Verzulli states in col. 3, line 4 that the EEPROM contains a manufacturer/model code. The difference between Verzulli and the claimed invention, in terms of the problem to be solved, is that Verzulli only stores one manufacture code while the claimed invention is capable of testing a plurality of brand names. Confronted with such a problem, a

skilled artisan would search for prior art that teach method for handling a plurality of brand names or manufacturers. Kamon et al. is such a prior art that teaches storing of a plurality of manufacturers in memory and selecting an appropriate one for operation. Kamon et al. teaches in col. 2, lines 60-66 storing command signals for instructing predetermined operations associated with a plurality of manufacturers. Chiloyan is another example, which teaches in col. 4, lines 45-55 storing settings for various models, brands or types of devices so that the same controller 12 and transmitter 18 can be used for controlling devices of the various brands. Such approach eliminates the need of different microcontrollers for different infrared transceivers. In other words, a single so-called "universal" microcontroller can be used for any brand names whose driving parameters have been stored in memory. Such combination of Kamon and Verzulli is desirable because it allows the use of a single microcontroller to test infrared transceivers made by various manufacturers, as recognized by Kamon and explained in col. 1, lines 25-33 of Kamon. Without knowing the brand name of a transceiver, the combination also allows the selection of appropriate driving setting based on self-test results by trying settings for different brand names and choosing the one that gives the best performance.

In summary, a skilled artisan, when confronted the problem of how to test an infrared transceiver using different brand name settings, one setting at a time, would have been motivated to extend the system and method of Verzulli by storing a plurality of settings for transceivers of different brand names in memory, as taught by Kamon or Chiloyan, and selecting one setting at a time for self-test because such combination allows the same controller to be used for testing transceivers of different brand names.

One pages 6-7 of the Brief, the Appellant cites col. 3, lines 15-30 of Verzulli, where flowing of data is described sequentially, and argues that in Verzulli's method, the transmission of test data and receiving of test data are conducted sequentially. To understand whether the transmission of test data and receiving of test data are conducted concurrently or not in Verzulli's method, an understanding of remote control that are used for electronic equipment such as TV and VCR (see col. 1, lines 15-17) is helpful. Verzulli teaches in col. 3, lines 47-53 the format of the self-test code. We can assume that a self-test code consists of around 80 bits. However, Verzulli does not teach how fast data bits are transmitted. It is well known in the art that data rates for remote control are in the order of 10 K bit per second (bps). For example, Umeda (U.S. Patent 5,737,107) shows in FIG. 3B that it takes 3 ms for a data stream of 21 bits, i.e., a data rate of 7 Kbps. Therefore, a self-test code of 80 bits occupies an interval of 8 ms, or it takes 8 ms for sending the complete sequence of the self-test code. On the other hand, Verzulli teaches a mirror for reflecting transmission data to the photodiode. If we assume a round trip distance of 3 meters for data from the transmitter to the receiver and a light speed of $3x10^8$ meters/second, the first bit arrives at the receiver at 10 ns after it has been transmitted. That is, when the receiver receives the first bit of the test data, the transmitter is still in the process of transmitting data. More specifically, at the beginning 10 ns, there is only transmission of test data, then both transmission and receiving occur simultaneously for the next 7.99999 ms. After the transmission of test data has been complete, receiving of test data lasts for another 10 ns. Even through Verzulli describes the flow of test data sequentially, it is understood that each step takes a certain period of time to finish and there is a good portion of time that transmission of test data and receiving of test data occur concurrently.

Furthermore, the remote controller of Verzulli incorporates both an infrared transmitter 18 and an infrared receiver 20. Therefore, it is capable of transmitting test data and receiving test data at the same time.

The Appellant states on page 7 of the Brief, "Two groups of direct access memory devices 510 and 520 are provided in the infrared controller 100 of the present invention for simultaneous data transmission and data reception." It appears that Appellant uses this structural feature to distinguish instant invention from the prior art. However, Verzulli teaches in col. 3, lines 35-38 that the CPU compares the content of the digitalized IR signal to the self-test code, which implies that the self-test code is stored in one place of memory (not necessary direct access memory) and the digitized (received) IR signal is stored in another place of memory. Please note that claim 1 only recites the function corresponding to this structural feature and does not recite the structure limitation. As discussed above, Verzulli fully supports the concurrency limitation.

The Appellant argues on pages 8-9 of the Brief that the problem to be solved by Weber is different not only from that of any one of Verzulli, Kamon and Chiloyan, but from the present invention as well, and concludes that there is no desirability (or a motive) disclosed in any one of Verzulli, Kamon (or Chiloyan) and Weber, for any one skilled in the art to which the invention pertained to make their combination because this combination does not benefit him/her. The problem to be solved by the additional limitation of claim 4 can be interpreted as a memory management problem. It is well known in the art that concurrency implies that the microprocessor runs multiple applications at the same time (e.g., see Microsoft Press Computer Dictionary, item "concurrent"). It is a common practice to divide memory into areas and allocate

each application its own memory area. Weber teaches in FIG. 9A such approach. The approach ensures each application has adequate memory which will not be overwritten by other applications. One of ordinary skill in the art, when confronted with the problem of multitasking would search for memory management strategy and would have been motivated to divide memory into different areas and assign different areas to different applications so that memory content will not be accidentally overwritten or corrupted by other applications.

The Appellant argues on pages 10-11 that there is no desirability (or a motive) disclosed in any one of Verzulli, Kamon (or Chiloyan) and admitted prior art for any one skilled in the art to which the invention pertains to make their combination because this combination does not benefit him/her. The Examiner disagrees. Verzulli teaches to use microcontroller for controlling the self-test. A South Bridge chip is just a special kind of controller that can be found in personal computers or other computer-based apparatus. South Bridge is commonly used with North Bridge; together, they are known as a chipset used in computers for controlling peripheral devices. (See, e.g., http://en.wikipedia.org/.) Infrared transceivers are used in computers for peripheral devices such as cordless keyboard or mouse. It is desirable to share the South Bridge controller among an infrared transceiver and other peripheral devices such as printer and modem, as taught by admitted prior art, because sharing keeps the cost of a computer low while provides additional functionality.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

skl

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